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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/510,567	10/08/2004	Hirohisa Miyazawa	029267.55488US	9020

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EXAMINER	
DINH, TUAN T	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/510,567	MIYAZAWA, HIROHISA	
	Examiner	Art Unit	
	Tuan T. Dinh	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/08/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/08/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 2, 4-8 are objected to because of the following informalities:

Claims 2 and 4, line 1, change "A circuit board device" to - - The circuit board device - - for proper antecedence basis..

Claims 4-8, line 1, change "A multilayer module board" to - - The multilayer module board - - for proper antecedence basis.

Claim 4, lines 8-9, is unclear. The phrase of "the base board...module board" is not understood because the multilayer module board is defined as one of "low end, high speed, or advance function module boards, please, correct.

Claim 6 is unclear because the phrase of "***assuming***...edge thereof" is not positive limitation. The term "assuming" is as prediction and does not positive shown a structure, please correct.

Claim 9, line 6 is unclear because the phrase of "***assuming***...edge thereof" is not positive limitation. The term "assuming" is as prediction and does not positive shown a structure, please correct.

Claim 10, line 6 is unclear because the phrase of "***assuming***...edge thereof" is not positive limitation. The term "assuming" is as prediction and does not positive shown a structure, please correct.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 4-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Taylor et al. (U.S. Patent 5,825,630).

As to claim 1, Taylor et al. discloses a circuit board device as shown in figures 1-2 comprising:

a base board (10, column 3, line 3) having a plurality of low-frequency electronic components; and

a multilayer module board (12, column 3, line 4) mounted at one surface of the base board and having a plurality of high-frequency electronic components (14, 16, column 3, lines 6-7) including at least a CPU and a memory, wherein

the multilayer module board is smaller in size than the base board (see figure 1), the plurality of high-frequency electronic components are wired to one another through a wiring pattern at an inner layer.

As to claim 4, Taylor et al. discloses the multilayer module board (12) is a high-speed module board that operates at higher speed than the low-end module board.

As to claim 5, Taylor et al. discloses the multilayer module board (12) comprising a plurality of high-frequency electronic components (14, 16) including a CPU and a memory mounted at, at least, a surface thereof, wherein: the plurality of high-frequency

electronic components are connected with one another through a wiring patterns formed at an inner layer thereof.

As to claims 6-8, Taylor et al. discloses the module board (12) and ***assuming*** an overall shape of a rectangle and having connector terminals provided as separate members each soldered onto one of four peripheral edges thereof.

As to claim 9, Taylor et al. discloses a multilayer module board (12) as shown in figures 1-2 comprising:

a plurality of high-frequency electronic components (14, 16) including a CPU and a memory mounted at, the plurality of high-frequency electronic components are connected with one another through a wiring pattern formed at an inner layer thereof; Taylor et al discloses ***the multilayer module board assumes*** an overall shape of a rectangle and has connector terminals provided as separate members each soldered onto one of four peripheral edges thereof; the four connector terminals each include a narrow, elongated base portion constituted of resin and a plurality of pins fixed to the base portion; and after the four connector terminals are each carried with the base portion attached to a transfer adapter, the four connector terminals are connected through soldering onto a rear surface of the board while attached to the transfer adapter.

As to claim 10, Taylor et al. discloses a multilayer module board (12) as shown in figures 1-2 comprising:

a plurality of high-frequency electronic components (14,16) including a CPU and a memory mounted at, the plurality of high-frequency electronic components are

connected with one another through a wiring pattern formed at an inner layer thereof; ***the multilayer module board of Taylor assumes*** an overall shape of a rectangle and has connector terminals provided as separate members each soldered onto one of four peripheral edges thereof; the four connector terminals each include; a narrow, elongated base portion constituted of resin; a plurality of pins fixed to the base portion; aligning pins projecting at both ends of the base portion to be used when soldering the connector terminal onto a rear surface of the board; and inclined surfaces for position control formed at both ends of the base portion to be used when soldering the connector terminal; a pair of positioning holes at which the aligning pins are loosely fitted are formed at each of four corners of the board; and positions of the connector terminals are controlled when soldering the connector terminals as the inclined surfaces for position control at adjacent connector terminals come into contact with each other while the positioning pins are loosely fitted at the positioning holes.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-3, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor et al. ('630) in view of Aruga et al. (U.S. Patent 6,085,137).

As to claim 2, Taylor et al. discloses at least a graphics circuit in addition to the CPU and the memory as shown in figure 1, is mounted at the multilayer module board, except for at least a power circuit, a gyro and a GPS circuit are mounted at the base board and device being used in a navigation system.

Aruga et al. teaches a vehicle control device (1) as shown in figure 1 comprising a navigation system (10) comprising at least a power circuit, a gyro and a GPS circuit are mounted at the base board.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a teaching of Aruga et al. employed in the device of Taylor et al. in order to provide information and detecting road for the vehicle.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Leicht et al., Begis, and Yasuho et al. disclose related art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tuan Dinh
August 28, 2006.